IN THE CLAIMS

Please amend the claims as follows:

1-32. (Canceled)

33. (Previously Presented) A semiconductor device comprising:

a delay circuit adapted to be supplied with a clock signal and delay the clock signal; and

a logic circuit adapted to be supplied with an output signal of said delay circuit and said clock signal,

said delay circuit including:

a capacitor connected to an output terminal of an inverter circuit, said capacitor being charged and discharged in response to the operation of said inverter circuit; and

a transistor connected between said capacitor and the output terminal of said inverter circuit, said transistor being turned off in response to the discharge of the capacitor.

34. (Previously Presented) The device according to claim 33, wherein said capacitor is inserted between the output terminal of said inverter circuit and ground, and said transistor is a P-channel MOS transistor.

35. (Previously Presented) The device according to claim 33, wherein said capacitor is inserted between the output terminal of said inverter circuit and a power source, and said transistor is an N-channel MOS transistor.

36. (Previously Presented) The device according to claim 34, wherein said capacitor is a MOS capacitor.

37. (Previously Presented) A semiconductor device comprising:

a delay circuit which delays an input signal;

first and second latch circuits which alternatively hold an output signal of said delay

circuit in response to a clock signal, said second latch circuit being adapted to supply the signal held in the second latch circuit to said delay circuit;

said delay circuit including:

an inverter circuit which receives the output signal of said second latch circuit; and

a capacitor connected to an output terminal of said inverter circuit, said capacitor being charged and discharged in response to the operation of said inverter circuit.

38. (Previously Presented) The device according to claim 37, wherein said first latch circuit is a first flip-flop circuit formed by using two NAND circuits.

39. (Previously Presented) The device according to claim 37, wherein said second latch circuit is a second flip-flop circuit formed by using two NOR circuits.

40. (Previously Presented) The device according to claim 37, wherein said second latch circuit is a third flip-flop circuit formed by using two NAND circuits, said third flip-flop circuit having first and second input terminals, said first input terminal being adapted to be supplied with an inverted clock signal, said second input terminal being adapted to be supplied with an inverted output signal of said first flip-flop circuit.

41. (Previously Presented) The device according to claim 40, wherein said third flip flop circuit includes a 3-input NAND circuit and the output signal of said inverter circuit is directly supplied to the first input terminal of said 3-input NAND circuit.

42. (Previously Presented) The device according to claim 37, wherein said first and second latch circuits are master/slave type delay flip-flop circuits.

43. (Previously Presented) The device according to claim 37, further comprising:

a transistor connected between the output terminal of said inverter circuit and the capacitor, said transistor being turned off in response to the discharge of the capacitor.

44. (Previously Presented) The device according to claim 37, wherein said capacitor is inserted between the output terminal of said inverter circuit and ground, and said transistor is constituted by a P-channel MOS transistor.

45. (Previously Presented) The device according to claim 37, wherein said capacitor is a MOS capacitor.

46. (Previously Presented) The device according to claim 37, further comprising:

a memory cell array including a plurality of memory cells arranged in rows and columns, said memory cells being connected to bit lines and word lines;

a sense amplifier connected to said bit lines of said memory cell array, said sense amplifier being adapted to sense and amplify the potentials of said bit lines;

a column selection gate which connects said sense amplifier to a first data line;

a word line selection circuit which selects the word lines; and

a column selection circuit which selects the column selection gate, wherein the column selection circuit is supplied with an output signal from a logic circuit.

47. (Currently Amended) The device according to claim 37, further comprising:

a memory cell array including a plurality of memory cells arranged in rows and columns, said memory cells being connected to bit lines and word lines;

a sense amplifier connected to said bit lines of said memory cell array, said sense amplifier being adapted to sense and amplify the potentials of said bit lines;

a column selection gate which connects said sense amplifier to a first data line;

a word line selection circuit which selects the word lines; and

a column selection circuit which selects the column selection ~~age~~ gate, wherein the column selection circuit is supplied with an output signal from the second latch circuit.